Subject (course) name: **Logic Circuits**		
Programme: **Computer Science** Specialty:		Subject code: **10K**
		Title graduate: **Engineer**
Type of course: **obligatory**	Course level: **First-cycle studies**	Year: **II** Semester: **III** Semester: **winter**
Form of classes: **Lectures, Classes, Labs, Seminar, Project**	Number of hours per week: **1L, 0, 2Lab, 0, 0**	Credit points: **4 ECTS**

GUIDE TO SUBJECT

SUBJECT OBJECTIVES

C1. General knowledge in analysis and synthesis of combinatorial and sequential logic circuits.

C2. General knowledge in the methods of modelling logic circuits and reasoning about their behaviour based on computer simulations.

C3. General skills in design and modelling logic circuits.

SUBJECT REQUIREMENTS

1. General knowledge in DC electrical circuits.
2. General knowledge in math particularly in Boolean algebra.
3. The ability to work independently and ability to work in a group.
4. The ability to write reports on laboratory exercises.
5. General ability to independently search in literature and online resources.

LERNING OUTCOMES

EK 1 – Student has a basic knowledge in combinatorial and sequential logic.

EK 2 – Student can distinguish and characterize logic device basing on verbal description, tables, canonical and standard forms or state diagrams;

EK 3 – Student can indicate elements needed to design an assumed logic circuit on the basis of a functional description, design or merge them into one circuit;

EK 4 – Student can perform the laboratory exercises examining real logic devices and simulate their operation by computerized simulators;

EK 5 – Student can interpret the results of simulations and examination of real logic devices.

SUBJECT CONTENT

Form of classes – lectures

Topic	Hours
W 1 – Boolean algebra	**1**
W 2 – Number representations, basic arithmetic operations	**1**
W 3 – Realization of ADC and DAC converters	**1**
W 4 – Gray code, Karnaugh maps, simplification of Boolean functions	**1**
W 5 – Realization of combinatorial logic by gates	**1**

W 6 – Decoders and encoders	**1**
W 7 – Multiplexers and demultiplexers	**1**
W 8 – Synthesis of the combinatorial logic, hazards	**1**
W 9 – Quine and McCluskey minimalization	**1**
W 10 – Flip-flops	**1**
W 11 – Synchronous sequential logic	**1**
W 12 – Moore and Mealy machines, realization of synchronous sequential logic by flip-flops	**1**
W 13 – Asynchronous sequential logic, critical races	**1**
W 14 – Memories – parameters and application	**1**
W 15 – TTL and CMOS technologies Final test	**0.5** **0.5**
Total	**15**

Form of classes – laboratory

Topic	Hours
L 1 – Introduction to program Multisim	**2**
L 2 – Study of logic gates	**2**
L 3 – Study of ADC	**2**
L 4 – Study of DAC	**2**
L 5 – Study of flip-flops	**2**
L 6 – Design and simulation of combinatorial logic circuits	**2**
L 7 – Study of multiplexers and demultiplexers	**2**
L 8 – Study of arithmetic circuits	**2**
L 9 – Study of arithmetic logic unit ALU	**2**
L 10 – Design a asynchronous and synchronous counters	**2**
L 11– Study of IC counters	**2**
L 12 – Races and hazards	**2**
L 13 – Study of IC registers	**2**
L 14 – Design and simulation of synchronic state-machine	**2**
L 15 – A colloquium	**2**
Total	**30**

STUDY METHODS

1. Lectures using multimedia presentations and computer arithmetic tasks
2. Discussion during the course and in addition during individual consultations
3. Laboratory – teamwork, design and simulation of logic circuits

EDUCATIONAL TOOLS

1. Audiovisual equipment, black(white)board
2. Set of laboratory stands
3. Instructions to laboratory stands
4. Multisim simulation environment

METHODS OF ASSESMENT (F – Forming, P – Summary)

F1. assessment of self preparation for laboratory classes – oral answer
F2. assessment of the correctness and timeliness of presentation software created
P1. lecture – written test of the theory
P2. assessment of knowledge acquired during the laboratory exercises (80% – labs)
P3. assessment of ability to solve problems, design circuits and result reporting (20% - labs)

STUDENT WORKLOAD

Form of activity		Averaged workload (hours)		
		[h]	∑ [h]	ECTS
Participation in class activities	lecture	15	48	2
	laboratory	30		
	consultation	3		
Preparation for tutorials (reading literature)		15		
Preparation for final test		15		

Preparation for a colloquium	15	52	2
Familiarizing yourself with the educational software	8		
Total		**100**	**4**

A. BASIC READING

1. Mano M., Ciletti M.: Digital Design, 4th-edition, Prentice Hall, 2007.

2. Godse D., Godse A.: Digital Logic Circuits, Technical Publications, 2008.

3. Cyran K., Pochopień B., Stanczyk U.: Theory of Logic Circuits. / Vol. 1 ; Fundamental Issues, Publ. House of Silesian University of Technology, 2007.

4. Nelson V., Nagle H.: Digital logic circuit analysis and design, Prentice Hall, 1995.

B. FURTHER READING

1. Holdsworth B., Woods C.: Digital Logic Design, Newnes 2002.

2. Langholz G., Kandel A., Mott J., William C. Brown 1988.

3. Rafiquzzaman M.: Fundamental of Digital Logic and Microcomputer, John Willey and Sons 2005.

Learning objectives	In relation to the learning outcomes specified for the field of study	Subject objectives	Study methods	Methods of assessment
EK1	K_W07 K_U13	C1	lectures, laboratory, discussion	P1
EK2	K_W07	C1	lectures, laboratory, discussion	P1,P2
EK3	K_W07	C2,C3	lectures, laboratory, discussion	F1,P2,P3
EK4	K_W05 K_U02 K_U13	C2,C3	laboratory, discussion	F1,F2,P2,P3
EK5	K_W13 K_U07	C2,C3	laboratory, discussion	F2,P2,P3

II. EVALUATION

Grade	Outcome
EK1	**Student has a basic knowledge in combinatorial and sequential logic**
2 (F)	Student has no knowledge in combinatorial and sequential logic
3 (E)	Student has a very elementary knowledge in combinatorial and sequential logic
4 (C)	Student has a basic knowledge in combinatorial and sequential logic and can draw schematics
5 (A)	Student has a basic knowledge in combinatorial and sequential logic and can draw schematics and also describe the rule of operation
EK2	**Student can distinguish and characterize logic device basing on verbal description, tables, canonical and standard forms or state diagrams**
2 (F)	Student can not distinguish and characterize logic device basing on verbal description, tables, canonical and standard forms or state diagrams
3 (E)	Student can distinguish and characterize logic device basing on verbal description, tables
4 (C)	Student can distinguish and characterize logic device basing on verbal description, tables, canonical and standard forms
5 (A)	Student can distinguish and characterize logic device basing on verbal description, tables, canonical and standard forms or state diagrams
EK3	**Student can indicate elements needed to design an assumed logic circuit on the basis of a functional description, design or merge them into one circuit**
2 (F)	Student can not indicate elements needed to design an assumed logic circuit on the basis of a functional description, design or merge them into one circuit
3 (E)	Student can indicate elements needed to design an assumed logic circuit on the basis of a functional description
4 (C)	Student can indicate elements needed to design an assumed logic circuit on the basis of a functional description merge them into one circuit
5 (A)	Student can indicate elements needed to design an assumed logic circuit on the basis of a functional description, design or merge them into one circuit

EK4	**Student can perform the laboratory exercises examining real logic devices and simulate their operation by computerized simulators**
2 (F)	Student can not perform the laboratory exercises examining real logic devices and can not simulate their operation by computerized simulators
3 (E)	Student can perform the laboratory exercises examining real logic
4 (C)	Student can perform the laboratory exercises examining real logic devices and can simulate chosen devices by computerized simulators
5 (A)	Student can perform the laboratory exercises examining real logic devices and simulate their operation by computerized simulators
EK5	**Student can interpret the results of simulations or examination of real logic devices**
2 (F)	Student can not interpret the results of simulations and examination of real logic devices
3 (E)	Student can interpret the results of simulations real logic devices
4 (C)	Student can interpret the results of examination of real logic devices
5 (A)	Student can interpret the results of simulations and examination of real logic devices

III. OTHER USEFUL INFORMATION

1. All information for students on the schedule are available on the notice board and on the website: www.el.pcz.pl
2. Information on the consultation shall be provided to students during the first lecture and will be placed on the website www.el.pcz.pl
3. Terms and conditions of credit courses will be provided to students during the first lecture